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OCT 11 2006Wu *et al.*

Appl. No. 10/017,793

BEST AVAILABLE COPY***Amendments to the Specification***

1. Please replace the paragraph beginning at page 8, line 21, which starts with "In another embodiment of the invention", with the following amended paragraph:

In another embodiment of the invention, a computer 170 may include a first processor 172 with a first (main) pipeline 105 having a data cache 110 coupled to a memory 122, and an instruction cache 115. The computer 170 may also include a second (run-ahead) pipeline 120 coupled to the data cache 110 and the instruction cache 115, as well as a data value prediction module 150 coupled to the run-ahead pipeline 120 (which may be included in a second processor 174). Alternatively, both pipelines 105, 120 may be included in a single processor 175, which may be coupled to a memory 122, 122' using a bus 123, 123'. As noted previously, a value prediction table 155 may be coupled to the value prediction module 150. A misprediction counter 162 and/or a run-ahead counter 165 may also be couple to the run-ahead pipeline 120, as part of a synchronization mechanism 160.